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[54] **STATE DEPENDENT SYNCHRONIZATION CIRCUIT WHICH SYNCHRONIZES LEADING AND TRAILING EDGES OF ASYNCHRONOUS INPUT PULSES**

[75] Inventors: **Jerald Alston**, Portola Hills; **Ting-Li Chan**, Laguna Niguel, both of Calif.

[73] Assignee: **QLogic Corporation**, Aliso Viejo, Calif.

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[52] **U.S. Cl.** **370/503**; 375/370; 375/354; 370/520

[58] **Field of Search** 375/354, 355, 375/356, 358, 360, 364, 370; 370/350, 503, 520; 327/141, 146, 154

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Primary Examiner—Chi H. Pham

Assistant Examiner—Frank Duong

Attorney, Agent, or Firm—Knobbe, Martens, Olson & Bear, LLP

[57] **ABSTRACT**

A state dependent synchronization circuit synchronizes an asynchronous input signal to a clock signal to generate a synchronous output signal. The circuit synchronizes both the leading edge and the trailing edge of the input signal and also maintains the state of the output signal at a level corresponding to the input signal when the input signal does not change. The circuit includes an input signal latch which receives the input signal and provides a latched signal which does not charge state even if the input signal subsequently changes state until the latched signal is synchronized to the clock signal. The circuit further includes a synchronizer which synchronizes the latched signal with the clock signal. The synchronizer provides feedback signals to the input signal latch to permit the input signal latch to recognize a change in the state of the input signal only after the synchronizer has synchronized the previous state of the input signal. The synchronizer preferably includes a first stage and a second stage. The first stage of the synchronizer isolates the second stage from any oscillation which may occur if the latched signal changes state too close to a transition in the clock signal. The first stage and the second stage of the synchronizer preferably operate on opposite edges of the clock signal. The circuit preferably includes a pair of cross-coupled gates that enable the circuit to recognize and synchrinize pulses of very short duration.

12 Claims, 3 Drawing Sheets