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[54] APPARATUS FOR DETERMINING CACHEABILITY OF A MEMORY ADDRESS TO PROVIDE ZERO WAIT STATE OPERATION IN A COMPUTER SYSTEM

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[57] **ABSTRACT**

A computer system includes an Intel 80486 microprocessor having an internal cache memory and a local memory tightly coupled to the microprocessor that can respond to memory accesses without requiring the microprocessor to execute a wait state. An external cache memory system is provided to provide additional cache storage to provide copy back capabilities so that data written to the external cache does not have to be automatically written to slower bulk memory. The computer system includes a conventional Industry Standard Architecture bus (ISA-bus) which may include memory on the bus. The computer system may also include an external math coprocessor. In order to preclude storing data from the math coprocessor and from the ISA-bus memory, the external cache memory system includes a cache determination circuit that selectively generates a cache enable signal to the microprocessor and to the external cache memory system so that only cacheable data is stored in the two caches. The cache determination circuit operates sufficiently fast that when the microprocessor addresses a zero-wait state device, such as the external math coprocessor or the local memory, a cache enable signal is generated within the first clock cycle so that the local memory can respond within the second clock cycle without requiring a microprocessor wait state and the cache enable signal is not generated if the math coprocessor is addressed.

3 Claims, 8 Drawing Sheets